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"A Simple EDDR architecture of motion estimation for Low power applications using FPGA"

Mis Shameena PM,

PG student,

Dept of Applied Electronics,

Er.Perumal Manimekhalai College of Engineering,

Hosur- 635 117, Krishnagiri district *Taminadu, India*

Mail id : shameenapm@gmail.com

Abstract

Using the integrated bandwidth Rate Distortion optimization framework, design of an efficient hardware architecture of Motion Estimation is made for resource-limited mobile video applications. This framework predicts and allocates the appropriate data bandwidth for motion estimation under a limited bandwidth supply to fit a dynamically changing bandwidth supply. A simple EDDR Architecture (Error Detection and Data recovery) is introduced in place of existing Motion estimation engine to reduce the power consumption. In existing design, ME engine performs motion estimation only, and was unable to detect and correct any type of errors in motion estimation process. Hence, we replace ME engine by EDDR architecture, which can generate motion vector with error correcting capabilities. In comparision with the previous low-complexity VLSI designs, the proposed work achieves good hardware utilization with reduced gate counts and requires only one-line memory

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buffer.The methodology uses Field Programmable GA with HDL Programming. Data recovery is made possible with less error rate. Also the Data can be recovered with less time delay.

Index Terms— FPGA Design, EDDR architecture, ME Engine, Low Power.

I- INTRODUCTION

Motion Estimation is the key component of motion compensation. During motion estimation, the motion of objects is measured and encoded into motion vectors. The search for the "best" motion vector requires that a criterion of optimality be defined. For example, motion vectors may be selected on the basis of maximum correlation or minimum error between macroblock pixels and the predicted pixels (or interpolated pixels for sub-pixel motion vectors) from the chosen reference frame. One of the most commonly used error measures is Mean Absolute Distortion (MAD)

$$MAD(x, y) = 1/mn \quad (1)$$

Where x and y are the coordinates of the upper left pixel of the m×n macroblock being coded, dx and dy are displacements from the reference frame as shown in Fig1, and p is an array of predicted macroblock pixel values. For sub-pixel motion vector estimation, p is interpolated from pixels in the reference frame. Typically, dx and dy must fall within a limited search region around each macroblock.Values from ±8 to ±64 pixels are common, and the horizontal search area often is slightly larger than the vertical area,A more computationally efficient error measure, called the Sum of Absolute differences (SAD), omits the 1/mn factor in eqn 1.

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Motion estimation is performed by searching for the dx and dy that minimize MAD(x,y) over the allowed range of motion vector displacements –including sub-pixel displacements. This process often is called block matching, an exhaustive search guarantees the best possible result, but is computationally expensive, because every possible motion must be tested over the entire displacement range 4225 16 × 16 MAD calculations is multiplied by a factor of 4 or 16, respectively. Fast search algorithms can reduce the computational burden but may or may not yield optimal motion vectors. A number of fast block-based motion estimation algorithms have been proposed and studied in the literature.

II- LITERATURE SURVEY

H.264/AVC standardization effort have been enhanced compression performance and provision of a "network-friendly" video representation addressing "conversational" (video telephony) and "non-conversational" (storage, broadcast, or streaming) applications. H.264/AVC has achieved a significant improvement in rate-distortion efficiency relative to existing standards[1]. To analyze, control, and optimize the rate-distortion (R-D) behavior of the wireless video communication system under the energy constraint, they have developed a power-rate-distortion (P-R-analysis framework, which extends the traditional R-D analysis by including another dimension, the power consumption. Specifically, in this paper, they have analysed the encoding mechanism of typical video coding systems, and develop a parametric video encoding architecture which is fully scalable in computational complexity[2]. a method to reduce the computation and memory access for variable block

size motion estimation (ME) using pixel truncation. Previous work has focused on implementing pixel truncation using a fixed-blocksize (16×16 pixels) ME. However, pixel truncation fails to give satisfactory results for smaller block partitions [3]. Video compression has become an essential component of broadcast and entertainment media. Motion Estimation and compensation techniques, which can eliminate temporal redundancy between adjacent frames effectively, have been widely applied to popular video compression coding standards such as MPEG-2, MPEG-4. Traditional fast block matching algorithms are easily trapped into the local minima resulting in degradation on video quality to some extent after decoding. In this paper various computing techniques are evaluated in video compression for achieving global optimal solution for motion estimation. Zero motion prejudgment is implemented for finding static macro blocks (MB) which do not need to perform remaining search thus reduces the computational cost. Adaptive Rood Pattern Search (ARPS) motion estimation algorithm is also adapted to reduce the motion vector overhead in frame prediction.

The simulation results showed that the ARPS algorithm is very effective in reducing the computations overhead and achieves very good Peak Signal to Noise Ratio (PSNR) values. This method significantly reduces the computational complexity involved in the frame prediction and also least prediction error in all video sequences. Thus ARPS technique is more efficient than the conventional searching algorithms in video compression[4].

III- PROPOSED METHOD

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A. Architectural implementation

The objective is to propose efficient hardware architecture for motion estimation design and to detect and reduce the errors in motion estimation process to improve the quality of the decompressed video – EDDR architecture which is being realized by ME Engine.We introduce Motion Vector error correction algorithm to enhance the video.

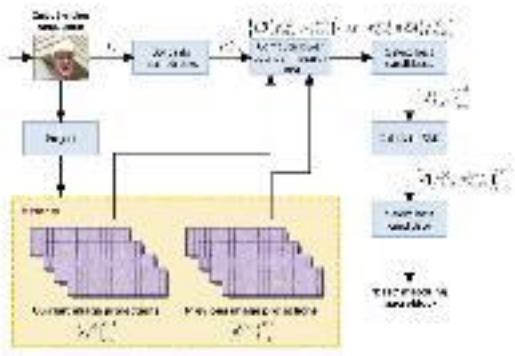

Fig 2 Motion Estimation Scheme

The algorithm is implemented through MATLAB software and simulated using ModelSim. Finally XILINX FPGA Navigator 9.2i for hardware synthesis using XCX3s500e. Verilog HDL is the hardware language used to synthesize the results.The input video is given as YUV video format which is the combination of luminance and chrominance. It is used because it can support color and gray scale image frames. The video we use is of QCIF resolution of 176 X 144. First frame is reference frame and second is the reference frame. The difference signal is manipulated.The algorithm is implemented and the input and

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calculated values. i.e., compression process can be viewed through the MODEL SIMulator, this simplifies the further design work post simulation in XILIINX Software.

The ME controller helps to achieve the following:

1. To allocate the Bandwidth of the current and reference frame.
2. To allocate the Bandwidth between the current and reference frame.
3. To determine the processing stage of the Motion Estimation Engine.

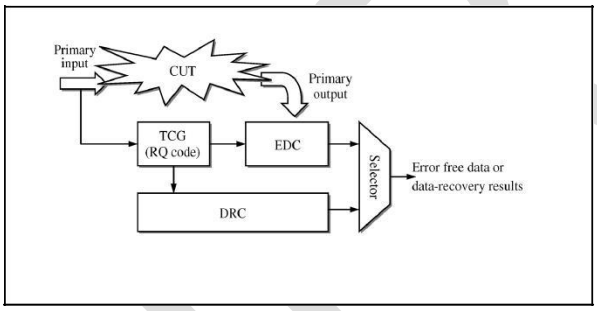

Fig.1. Eddr architecture

EDD scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data. It also consists of PE(Processing Elements) and test code generator(TCG). The test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the

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CUT has errors. DRC is in charge of recovering data from TCG.

B. TCG Design

TCG(Test code Generation) is an important component of the proposed EDDR architecture. TCG is used to generate corresponding test codes in order to detect errors and recover data. Each TCG Consists of RQ (residue-and-quotient)Code generator(RQCG) to generate residue-and-quotient.

TEST PATTERN GENERATION

CLK	QA^QC	Q-A	Q-B	Q-C	STWK-SEQ
	1	1	0	0	0

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1	1	1	1	0	0
2	0	1	1	1	1
3	1	0	1	1	1
4	0	1	0	1	1
5	0	0	1	0	0
6	1	0	0	1	1

C. Residue-and-Quotient Generation

The Processing Element generate the SAD(Sum of Absolute Difference) value. It estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macro block.We propose EDDR Architecture (Error detection and data recovery) in place of existing Motion estimation engine to reduce the power consumption.In existing design, ME engine performs motion estimation only, not able to detect and correct any type of errors in motion estimation process. In phase2, we replace ME engine by EDDR architecture ,which able to generate motion vector with error correcting capabilities.The

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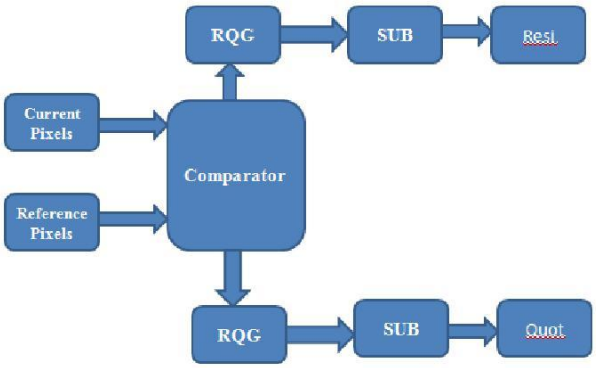
residue and quotient is generated randomly for all possible pixels in a video frame. The residue of the motion estimation and EDD circuitry is calculated as follows.

$$
\begin{aligned}
R_T &= \left| \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (X_{ij} - Y_{ij}) \right|_m \\
&= \left| |(X_{00} - Y_{00})|_m + |(X_{01} - Y_{01})|_m + \ldots \right. \\
&\quad \left. + \left| (X_{(N-1)(N-1)} - Y_{(N-1)(N-1)}) \right|_m \right|_m \\
&= \left| |(q_{x00} \cdot m + r_{x00}) - (q_{y00} \cdot m + r_{y00})|_m \right. \\
&\quad + \ldots \left| (q_{x(N-1)(N-1)} \cdot m + r_{x(N-1)(N-1)}) \right. \\
&\quad \left. \left. - (q_{y(N-1)(N-1)} \cdot m + r_{y(N-1)(N-1)}) \right|_m \right|_m
\end{aligned}
$$

The quotient of the processed pixels of the video frame is given by

$$
\begin{aligned}
Q_T &= \left\lfloor \frac{\sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (X_{ij} - Y_{ij})}{m} \right\rfloor \\
&= \left\lfloor \frac{(X_{00} - Y_{00}) + (X_{01} - Y_{01}) + \ldots + (X_{(N-1)(N-1)} - Y_{(N-1)(N-1)})}{m} \right\rfloor
\end{aligned}
$$



IV- RESULTS AND DISCUSSIONS

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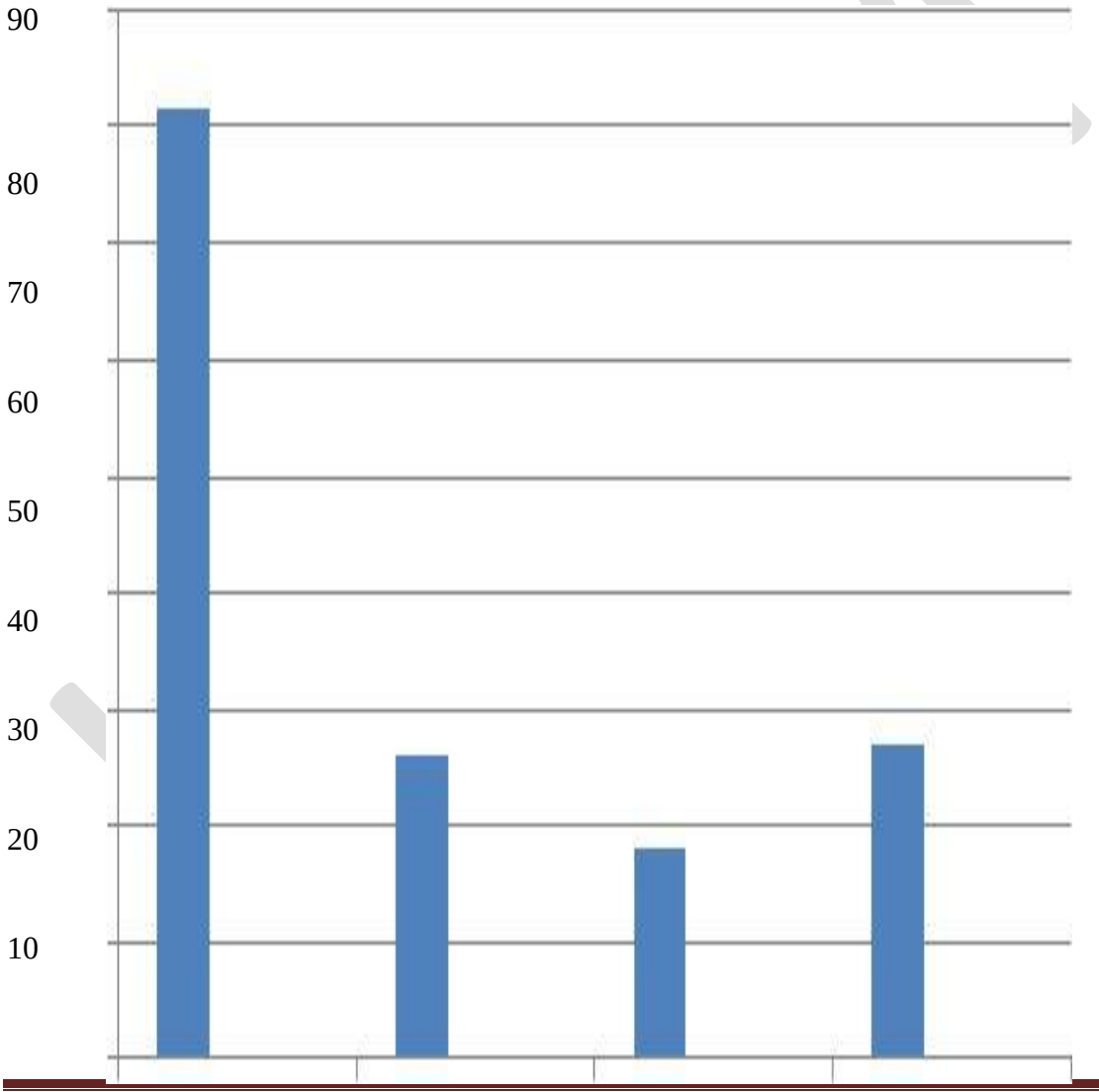
As the process is executed using Xilinx simulator too, the designed motion estimation circuit consumes 81.37mW of power consumption.



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0

Power C@1.2v C@2.5v JT

A final point is that when a VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic device such as a CPLD or FPGA, and then it is the actual hardware being configured, rather than the VHDL code being "executed" as if on some form of a processor chip.

Evaluation Parameters	**Results**
Power Consumption	81.37mW
Quiescent Current at 1.2v	26.15mA
Quiescent Current at 2.5v	18mA
Junction Temperature	27.94

Table 1 Power Analysis

Fig. 3.Performance analysis Graph

*Performance Analysis:*The table shows the comparison of existing and proposed design in terms of power consumption.

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Components	Existing Method(mw)	Proposed Method(mw)
PE	625	568

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RQCG	342	278
TCG	452	324
DRC	631	235

Fig 3.Simulation Results

V- CONCLUSION

Motion analysis is a computationally complex problem and need to process real scenes containing artifacts and even small targets. Algorithms need to operate on optimal features to derive clues regarding the type of motion executed. Through proper selection of efficient algorithms, FPGA design of low power high performance architecture for motion estimation is made successful with the advantages of Less Complex Architecture, Low power implementation. As a result, the final design can provide superior power efficiency under CIF and D1 30-frames/s video coding as compared to the previous state-of-the-art designs.

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